UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,749	06/26/2003	Andreas Schrader	00990088AA	3819

30743 7590 09/25/2007

WHITHAM, CURTIS & CHRISTOFFERSON & COOK, P.C.
11491 SUNSET HILLS ROAD
SUITE 340
RESTON, VA 20190

EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2616	

MAIL DATE	DELIVERY MODE
09/25/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/603,749	SCHRADER ET AL.	
	Examiner	Art Unit	
	Ian N. Moore	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 August 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/24/07* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on 8/24/07. FIG. 2-3 accepted by the examiner. However, in the Replacement FIG. 1, right hand portion of the FIG. 1 appears to be faded and the labels inside processing unit appear to be distorted. It is suggested to resubmit the replacement FIG. 1.

Claim Objections

2. Claims 1-18 are objected to because of the following informalities:

Claim 1 recites "**the** data" in line 3. For consistency and clarification with "time-synchronous data" recited in line 2, it is suggested to change ""**the** data" in line 3, to "**the** time-synchronous data ".

Claim 1 recites, "**adaption**" in line 10, and it is suggested to change to "adaptation".

Claim 2 recites "**the** setup and/or adaptation" in line 2. For consistency and clarification with "setup and adaptation" recited in claim 1, line 10, it is suggested to change ""**the** setup and/or adaptation" in line 2, to "**the** setup and adaptation".

Claims 3-18 are also objected since they are depended upon objected claim 1 as set forth above.

Appropriate correction is required.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required:

Claim 16 recites "**data load and** network characteristics" in line 2. The specification fails to provide the support for "data load" or "**data load and** network characteristic".

Claim 14 recites "a plurality of the second processing units is setup, and, **after switching by the switch, the subcomponents of the first processing unit are included in one of the second processing unit** " in line 1-2. The specification fails to provide the support for BOLD limitation.

Claim Rejections - 35 USC § 112 – First Paragraph

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 13 and 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. (*NOTE- these issues have been raised in previous office action*).

Claim 13 recites, "after switching by the switch, the subcomponents of the first processing unit are **de-attached from each other**" in line 1-2.

The specification fails to disclose how subcomponents (see FIG. 3, 6a',6b', 6c') of processing unit 3 are de-attached after switching to processing unit 4. In other word, CODEC 6a', FILTER 6b' and PACKTIZER 6c' in the processing unit 3 are disconnected to each other after switching. The specification page 6-7 repeatedly discusses processing unit 3 and unit 4 are performing parallel by togging the switch between processing units in order to adapt to the changed data rate network characteristic. It is unclear how CODEC 6a', FILTER 6b' and PACKTIZER 6c' disconnected from each other after switching. Are they are actually removed? How does the disconnection occur between CODEC, FILTER and PACKTIZER? How does the processing unit 3 operate after essential components such as CODEC, FILTER and PACKTIZER are de-attached (e.g. processing time sensitive data packet without CODEC, FILTER, or PACKTIZER)? How disconnected CODEC, FILTER and PACKETER can perform parallel processing, if they are disconnected? What is the relationship between the resources and subcomponents? How do the subcomponents de-attached after switching with regards to resources?

Applicant responded to this issue recited the previous action by referring page 9, lines 29 to 33, which contain neither explanation nor support claimed invention. Applicant referred page and lines or any other pages provide the support for the claimed invention. The specification recites on page 9, "***in order to allow for particular good exploitation of resources, the subcomponents of the processing unit could be de-attached after switching***". This recitation does not explain the questions set forth above, and it merely repeats the clam.

Applicant responded to this issue recited in the previous by arguing that examiner assuming is incorrect (in applicant remarks page 12), yet the applicant fails to clearly point out the enabling reference in the specification where the claimed invention is supported. What appears to disclose by the applicant specification and figures, is as follows: after switching, the first processing subcomponents (6a', 6b',..) are de-attached/separated from the second processing subcomponents (7a',7b',...). Since the applicant was unable to clearly point out the enabling reference in the specification, examiner sustains the assumption, for the purpose of the examination, "in light of the applicant disclosure" *that after switching, the first processing subcomponents (6a',6b',..) are de-attached/separated from the second processing subcomponents (7a',7b',...).*

Claim 14 recites, "**the** subcomponents of the first processing unit **are included in one of the second processing units**" in line 2-4.

The specification fails to disclose how subcomponents (see FIG. 3, 6a',6b', 6c') of processing unit 3 are included in the processing unit 4 after switching by the switch. Per FIG. 3, the processing unit 4 already have subcomponent CODEC 7a, FILTER 7b and PACKETIZER 7c, and then one of CODEC 6a, FILTER 6b and PACKETIZER 6c is included in the second processing unit. It is unclear how the second processing unit uses two CODECs, two FILTERs, or two PACKTIIZER. How does one process using one of CODEC 6a, FILTER 6b and PACKETIZER 6c, with existing CODEC 7a, FILTER 7b and PACKETIZER 7c? How do they integrate? The specification page 6-7 repeatedly discusses processing unit 3 and unit 4 are performing parallel by togging the switch between processing units in order to adapt to the changed data rate network characteristic. It is unclear what kind of parallel processing can

possible done when CODEC 6a, FILTER 6b and PACKETIZER 6c in the processing unit 3 is included in the processing unit 4. What is the relationship between the resources and subcomponents? What resources which are not currently being used returned to the system for re-use? What is the system- processing unit 1 or 2? How does resource reuse by the system?

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 1-4 and 6-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zahn (WO 00/62254) in view of Botzko (US005983192A).

Regarding Claim 1, Zahn discloses an apparatus (see FIG. 1,2; apparatus 1) for the transmission of time-synchronous data (see FIG. 3, video signal 50; see page 4, paragraph 3-8; see page 9, last paragraph; real time/synchronous video signal utilizing MPEG or HDTV) from a sender to a receiver using a network (see page 4-6; a video signal must transmit from a transmitter to a receiver/customer over a network), wherein the data is processed and transmitted at the sender as well as the receiver (see FIG. 1, 2,4,5, the video data is processed at transmitter or receiver/customer; see page 9, last paragraph), the mechanism comprising:

a first processing unit (see FIG. 1, 2,4,5, a combined system of Processor CPU 5 and memory 6; see page 9, last paragraph), and a second processing unit parallel to the first processing unit (see FIG. 1,2, 4,5, a combined system of Processor CPU 5' and memory 6',

where a combined system of CPU 5 and memory 6 is parallel to a combined system of CPU 5' and memory 6'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2 to page 13, paragraph 2), wherein the second processing unit is setup and adapted based on changed sender data rata or network characteristics (see page 4, paragraph 3-4, page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6, last paragraph; CPU 5' is setup and fit/adapted for parallel processing according to sender/transmitter/source increasing/changing real time data rate (i.e. data rate 4 or 8 times/factor of 25/30 frames/second that carriers high resolution format), or real time data load or bandwidth/delay (i.e. network characteristic)), wherein data processing and transmission of the time-synchronous data is continued within the first processing unit during the setup and adaptation of the second processing unit (see page 11, paragraph 1-3; processing and transmission of real time data packet (e.g. packet 101) is continued/parallel-processed in the CPU 5 while CPU 5' is setup and fit/adapted for parallel processing); and

selecting/switching between the first and second processing units (see FIG. 1, line 2, switching/changing/selecting between CPU 5 and CPU 5'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5), the processing and transmission of the time-synchronous data initially being performed by the first processing unit (see FIG. 2, processing and transmission of real time data packet primarily/initially performed by the CPU 5; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2 to page 13, paragraph 2) and after switching (see FIG. 1-3, after switching/changing/selecting), the processing and transmission of the time-synchronous data is performed using the second processing unit (see FIG. 1-3, processing and transmission of real time data packet (e.g. continue

data packet 102) is processed by CPU 5'; see page 4, paragraph 3-4, 8 page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6, last paragraph) such that the processing and transmission of the time-synchronous data is performed within the second processing unit (see FIG. 1-3, the pr processing and transmission of real time data packet (e.g. continue data packet 102) is processed by CPU 5'' see page 4, paragraph 3-4, 8 page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6, last paragraph).

Although Zahn discloses changing/selecting/switching between the first processing unit and the second processing units, Zahn does not explicitly disclose a switch.

However, it is well known in the art the selecting/changing/switching is performed by a switch/selector/changer. In particular, Sastry discloses an apparatus (see FIG. 2, server 220/230/260; see FIG. 3, server 310; see FIG. 4,6; server 405/605) for the transmission of time-synchronous data (see FIG. 2, real time data; see col. 3, line 29-31, 48-51, 62-67) from a sender (see FIG. 2, sending/transmitting client 241-244/251-254) to a receiver (see FIG. 2, receiving client 251-254/241-244) using a network (see FIG. 2, using network 210), wherein the data is processed and transmitted at the sender as well as the receiver (see FIG. 2,3,4,6, server 310 process and transmitted to sending client 241-244 as well as the receiving client 251-254; see col. 3, line 32 to col. 4, line 10) the mechanism comprising:

a first processing unit (see FIG. 4, DSP-S 431, see FIG. 6, DSP-S631, or see FIG. 8, DSP 801/802), and a second processing unit parallel to the first processing unit (see FIG. 4,6,8. DSP-D 439/639/803 parallel to DSP-S 431/631/801), wherein data processing and transmission of the time-synchronous data is continued within the first processing unit during the setup and

adaptation of the second processing unit (see col. 4, line 32-60; see col. 5, line 12-20; processing and transmission of real time data is continued/process-parallel in the DSP-S 431/631/801 while setting-up/construction and adapting/configuring DSP-D 439/639/803 for parallel processing) and

a switch selecting between the first and second processing units (see FIG. 4,6, switch 420/620), the processing and transmission of the time-synchronous data initially being performed by the first processing unit (see FIG. 4,6, 8, processing and transmission of real time data primarily/initially performed by the DSP-S) and after switching by the switch (see FIG. 4, 6, 8, after switching by a switch 420/620; see col. 4, line 39-62; see col. 5, line 10-26, 36-56; see col. 6, line 12-20l; see col. 6, line 55 to col. 7, line 11), the processing and transmission of the time-synchronous data is performed using the second processing unit such that the processing and transmission of the time-synchronous data is performed within the second processing unit (see FIG. 4,6,8, processing and transmission of real time data is performed using the DSP-D (or any another DSP besides DSP-S) such that processing and transmission of the real time data is performed within DSP-D (or another DSP); see col. 4, line 39-62; see col. 5, line 10-26, 36-56; see col. 6, line 12-20l; see col. 6, line 55 to col. 7, line 11).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide a switch, as taught by Sastry in the system of Zahn, so that it would increase the support for the number of simultaneous calls/real-time data transmission and efficient resource allocation; see Sastry col. 3, line 15-30; see col. 7, line 5-12.

Regarding Claim 2, Zahn discloses wherein the setup and/or adaptation of the second processing is started using a trigger event (see FIG. 1, PULL request 1 is used to being

processing video frames in CPU 5'; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4).

Regarding Claim 3, Zahn discloses wherein the switching is performed after the completion of the setup and/or adaptation of the second processing unit (see FIG. 2, switching/changing to CPU 5' after setup/configuration/setting CPU 5'; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 4, Zahn discloses wherein the switching is performed after reaching a certain switching condition (see FIG. 2, switching/changing to CPU 5' after frame 101 is processed by CPU 5; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 6, Zahn discloses wherein the time-synchronous data is processed in the first processing unit using a plurality of subcomponents (see FIG. 2, a first combined processing system comprising CPU 5 and memory 6; see page 12, paragraph 2).

Regarding Claim 7, Zahn discloses wherein the subcomponents includes at least one of a memory buffer (see FIG. 2, a first combined processing system comprising memory 6; see page 12, paragraph 2).

Regarding Claim 8, Zahn discloses wherein the time-synchronous data is processed in the second processing unit using a plurality of subcomponents (see FIG. 2, a second combined processing system comprising CPU 5' and memory 6'; see page 12, paragraph 2).

Regarding Claim 9, Zahn discloses wherein the subcomponents includes at least one of a memory buffer (see FIG. 2, a second combined processing system comprising memory 6'; see page 12, paragraph 2).

Regarding Claim 10, Zahn discloses wherein the subcomponents are connected during the setup (see FIG. 2, CPU 5' and memory 6' are connected during the configuration/setups; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 11, Zahn discloses wherein the first and second processing unit is initialized after the setup (see FIG. 2, a combined system of CPU 5/5' and memory 6/6' initialized/started/begin processing after the configuring/setting-up the each pipeline connections 1; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 12, Zahn discloses wherein each of the subcomponents of the second processing unit is adapted to the other subcomponents (see FIG. 2, CPU 5' and memory 6' of the combined system of CPU 5' and memory 6' is adapted/fit/adjust/corresponds to other CPU 5/5" and memory 6/6"; see page 12, paragraph 2), or the changed data rate, or changed network characteristics (see page 8, paragraph 3-7; page 11, paragraph 1 to page 12, paragraph 3; see page 13, paragraph 5-6; parallel processing accommodate/conform to the network dynamic/change nature of real time data rate or bandwidth/delay (i.e. network characteristics)).

Regarding Claim 13, Zahn discloses wherein after the switching process, the subcomponents of the first processing unit are de-attached from each other (see FIG. 2, after switching/changing to CPU 5', CPU 5 and memory 6 are separated/de-attached from CPU 5' and memory 6; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 14, Zahn discloses a plurality of the second processing units is setup and after switching by the switch (see FIG. 2, a second combined system of CPU 5' and memory 6' and a third combined system of CPU 5" and memory 6" are configured/setup, and after switching by the switch); and the subcomponents of the first processing unit (see FIG. 2, a first combined processing system comprising CPU 5 and memory 6; see page 12, paragraph 2). Sastry discloses a plurality of the second processing units is setup (see FIG. 8, DSP 803,504,805,806 are setup/configured/constructed) and after switching by the switch after switching by the switch, the subcomponents of the first processing unit are included in one of the second processing units (see FIG. 8, after switching by a switch 420/620, subcomponent 2 ADPCM (Adaptive Pulse Code Modulation for voice compressing) from DSP 801 (i.e. first processing unit) are now included in the DSP 803; see col. 6, line 55 to col. 7, line 10).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to subcomponents of the first processing unit are included in one of the second processing units, as taught by Sastry in the system of Zahn, for the same motivation as set forth above in claim 1.

Regarding Claim 15, Zahn discloses wherein after switching by the switch, the subcomponents of the first processing unit remain connected (see FIG. 2, after switching/changing to CPU 5', CPU 5 and memory 6 are still connected; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 16, Zahn discloses wherein a plurality of second processing units (see FIG. 2, a combined system of 5" and memory 6", and more pipelines 1) are setup and adapted based on changed data load and network characteristics (see page 9, last paragraph; see page 11,

paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5; third combined system of 5" and memory 6" or more pipelines are setup/configured to accommodate/conform to the network dynamic/change nature of real time data load or bandwidth/delay (i.e. network characteristics)).

Regarding Claim 17, Zahn discloses wherein an additional processing unit (see FIG. 2, a combined system of CPU 5" and memory 6") for the processing and/or transmission of time-synchronous data is used in sequence with the first and second processing units (see FIG. 2, a combined system of CPU 5" and memory 6" process the video data (i.e. processing of frame 103) in parallel sequence with first and second combined systems (i.e. processed frames 101 and 102); see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Regarding Claim 18, Zahn discloses wherein the time-synchronous data is gathered with one of mechanisms for acquiring visual data and speech data (see page 4, paragraph 3-8; see page 9, last paragraph; video data is collected/received by a apparatus 1 for obtaining/acquiring video data (i.e. image/visual data and audio/speech data).

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zahn and Sastry, and further in view of Muniere (US007095717B2).

Regarding Claim 5, Zahn discloses wherein the certain switching condition is whether at least one given parameter (see FIG. 2, switching/changing to CPU 5' or 5" is based on whether frame 101 is processed by CPU 5; see page 9, last paragraph; see page 11, paragraph 1-2; see page 12, paragraph 2; see page 13, paragraph 4-5).

Zahn does not explicitly disclose reaches at a predetermined value. However, Muniere teaches the certain switching condition (see FIG. 4, Switch 41) is whether at least one given parameter reaches at a predetermined value (see FIG. 3-4, switching is performed according to meeting threshold/maximum High/low priority data counts; see col. 5, line 4-55; see col. 6, line 26-45).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide switching when reaching a predetermined value, as taught by Muniere in the system of Zahn, so that it would provide guaranteeing a minimum time interval for transmission of data packets; see Muniere col. 6, line 40-45.

Response to Arguments

9. Applicant's arguments with respect to claims 1-18 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claims 13 and 14, the applicant argued that, "...examiner is referred to page 9, line 29 to 33, which provide the support for this feature...examiner assumption...is incorrect...as to claim 14, the examiner demonstrates a similar misconception...page 9 of the specification, that is, resources which are not currently being used are returned to the system for re-use ...it is respectfully submitted that the claims have been misinterpreted by the examiner. To aid the examiner in his reconsideration of the claims, the following comments are offered..." in page 12-15.

In response to applicant's argument, the examiner respectfully disagrees with the argument above. As set forth in U.S.C. 112, 2nd rejection above, the specification still fails to

provide support the claimed invention set forth in claim 13 and 14. Applicant statement of "resources which are not currently being used **are returned to the system for re-use**" is still unclear as to how resources are being return to the system for re-use. Please see 112, 1st rejection set forth above.

Applicant's comments to aid the examiner's understanding still have not addressed 112, 1st issue. Since the applicant comments are not the specification, and examiner will not consider the applicant comments as the support the claim 13 and 14.

Regarding claims 1-18, the applicant argued that, "...Zahn does not disclose transmission of time-synchronous data and certainly does not disclose transmission of data using a network...**This process is not real time**. Zahn is not transmitting data from a sender to a receiver. Muniere cannot be combined with Zahn to make a workable system. The two are in entirely different technical fields...There is no basis in fact for the conclusion of obviousness..." in page 11-15.

In response to applicant's argument, the examiner respectfully disagrees with the argument above.

Zahn discloses an apparatus (see FIG. 1,2; apparatus 1) for the transmission of time-synchronous data (see FIG. 3, video signal 50; see page 4, paragraph 3-8; see page 9, last paragraph; real time/synchronous video signal utilizing MPEG or HDTV) from a sender to a receiver using a network (see page 4-6; a video signal must transmit from a transmitter to a receiver/customer over a network), wherein the data is processed and transmitted at the sender as well as the receiver (see FIG. 1, 2,4,5, the video data is processed at transmitter or receiver/customer; see page 9, last paragraph).

Also, one skilled in the ordinary art will clearly see that MPEG/HDTV is a real time packet data, that is transmitted from a sender (i.e. MPEG/HDTV generator/transmitter) and to a receiver (i.e. MPEG/HDTV receiver/player) over a network. The "network" is consisted of sender, receiver and the apparatus that process the MPEG/HDTV video packets. Applicant has not claim any specification with regards to sender, receiver and network. When MPEG/HDTV video packets are created, it is clear that there is a sender/transmitter/generator, a receiver/player, and a network where transmission of the MPEG/HDTV video packets occur.

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., **the real time process**) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Even if this limitation is claimed, Zahn still discloses the real time procession of MPEG/HDTV video packets.

In response to applicant's argument that "*the two are in entirely different technical fields***"** (i.e. nonanalogous art), it has been held that a prior art reference must either be in the field of applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the applicant was concerned, in order to be relied upon as a basis for rejection of the claimed invention. See *In re Oetiker*, 977 F.2d 1443, 24 USPQ2d 1443 (Fed. Cir. 1992). In this case, the combined system of Zahn, Sastry and Muniere and the applicant's invention are concerted with the certain switching condition (see FIG. 4, Switch 41) is whether at least one given parameter reaches at a predetermined value (see FIG. 3-4, switching is performed

according to meeting threshold/maximum High/low priority data counts; see col. 5, line 4-55; see col. 6, line 26-45). Thus, it is clear that Muniere is the analogous art.

In response to applicant's argument, the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N. Moore whose telephone number is 571-272-3085. The examiner can normally be reached on 9:00 AM- 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on 571-272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ian N. Moore INM
Examiner
Art Unit 2616

9-5-07

DORIS H. TO
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600